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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,543	04/14/2004	Tomomitsu Risaki	S004-5271	8834

7590 12/17/2004

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,543	RISAKI, TOMOMITSU	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/14/2004 (filing)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 4/15/2003. It is noted, however, that applicant has not filed a certified copy of the Japanese application (2003-110629) as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. ***Claim 1*** is rejected under 35 U.S.C. 102(b) as being anticipated by Fu (6,436,798 B2). Fu et al teach (title, abstract, Figures 4A-D; and col. 2, l. 63 – col. 4, l. 35, especially col. 3, l. 53-57) a semiconductor device (cf. title) comprising: a semiconductor substrate 308 (col. 3, l. 55-56; Figure 4B); source/drain regions 304 and 306 (col. 3, l. 63 – col. 4, l. 2 and Figure 4A) that are separately provided on a surface portion of the semiconductor substrate (as evidenced from the top view offered by Figure 4A): a concave portion (along cross section C-C' in Figure 4A as depicted by Figure 4B) formed in a channel length direction (L is the length of the channel of the device and C-C' is along said channel length; cf. col. 3, l. 47-63) so as to lineally connect the source / drain regions (see Figure 4C) , a plurality of the concave portions being arranged in a channel width (W) direction (cf. Figure 4B and col. 3, l. 53-57); an

insulating film 302 (cf. col. 3, l. 56) provided on the surface of the semiconductor substrate including the concave portions between the source/drain regions (cf. Figures 4A-4C); and a gate electrode 300 (cf. col. 3, l. 59-64) provided on the insulating film. In conclusion Fu et al anticipate claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claim 2*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu (6,436,798 B2) in view of Coe 4,939,390). *As detailed above, Fu et al anticipate claim 1. Fu et al do not necessarily teach the further limitation as defined by claim 2. However, it would have been obvious to include said further limitation in view of the commonly applied depletion mode operation of MOSFET devices, in which the channel region is depleted upon application of a gate voltage (N.B.: this is, in light of the Specification, what Applicant means by 'depleted', as is evidenced from section [0014]), discussed for instance by Coe who advocates using MOSFETs in depletion mode (col. 6, l. 47-57). Motivation* to include the teaching by Coe is the specific teaching by Coe that depletion mode MOSFET devices have a higher threshold voltage and consequently the source current is independent of the variance in threshold voltage (col. 6, l. 31-46) while depletion mode MOSFETs are physically smaller than enhancement MOSFET devices, resulting in less parasitic capacitance (col. 6, l. 47-57).

6. ***Claim 3*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al (6,436,798 B2) in view of Arai (6,084,283). *As detailed above, Fu anticipates claim 1. Fu does not necessarily teach the further limitation as defined by claim 3. However, it would have been obvious to include said further limitation in view of Arai*, who, in a patent on high-voltage MOSFET devices (such as used for read and erase operations; see col. 1, l. 9-23), - hence closely related to the invention by Fu, teach the consolidation on one chip of a plurality of high-voltage MOSFET devices (PMOSFET and NMOSFET devices with gates marked 205 in Figure 7 or 405 in Figure 11 for instance) (cf. col. 2, l. 20-30) in the region marked HBA with a MOS transistor for a logic circuit unit in the region marked LBA (see also col. 28-33). *Motivation* to include the teaching in this regard by Arai in the invention by Fu derives from the well-known cost savings flowing from integrated circuitry combined with the diverse voltage requirements for writing/erasing versus reading functions performed by different transistors, the writing/erasing transistors having the higher voltage settings (cf. col. 1, l. 9-23) compared with those for reading functions (loc.cit.), as a result of which only the writing/erasing transistors need to be designed so as to decrease the short-channel effect (see Fu, abstract, final sentence).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Fu (US 2002/0089019 A1, US Patent Application Publication).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
December 12, 2004

Patent Examiner:

Johannes Mondt (Art Unit: 2826)